[Total No. of Questions - 9] [Total No. of Printed Pages - 3] (2125)

15114

B. Tech 4th Semester Examination

Computer Architecture (OS)

IT(ID)-4001

Time : 3 Hours **Max. Marks : 100**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : Attempt five questions in all selecting one question from each section A, B, C and D of question paper. Section E is compulsory.

SECTION - A

1. (a) What do you understand by benchmark suit? Explain how the Desktop benchmarks are used to evaluate the performance?

   (b) Explain Amdahl's Law. Suppose that we are considering an enhancement to the processor of a server system used for web serving. The new CPU is 10 times faster on computation in the web serving application than the original processor. Assuming that the original CPU is busy with computation 40% of the time and is waiting for I/O 60% of the time, what is the overall speedup gained by incorporating the enhancement? (5+10=15)

2. (a) Explain advantages and disadvantages of various type of Instruction Set Architecture (ISA).

   (b) Explain various addressing modes by taking suitable examples. (5+10=15)

[P.T.O.]

SECTION - B

3. (a) How to reduce branch cost with prediction?

   (b) How is pipelining implemented? Explain the concept and challenges of instruction-level parallelism. (5+10=15)

4. (a) What do you understand by branch penalties and how it can be reduced?

   (b) What is loop unrolling? How it is useful to implement instruction level pipelining (ILP)? Explain with suitable example. (5+10=15)

SECTION - C

5. (a) What are the policies used to replace a cache block on cache miss?

   (b) Assume we have a computer where the clocks per instruction (CPI) is 1.0 when all memory accesses hit in the cache. The only data accesses are loads and stores, and these total 50% of the instructions. If the miss penalty is 25 clock cycles and the miss rate is 2%, how much faster would the computer be if all instructions were cache hits? (5+10=15)

6. (a) Compare various type of storage devices.

   (b) Discuss briefly about buses connecting I/O devices to CPU memory with suitable diagrams. Explain about RAID. (5+10=15)

SECTION - D

7. (a) What are practical issues for commercial interconnection networks with suitable examples?

   (b) Explain centralized shared memory architecture with suitable diagrams. What are simple network interconnections? (5+10=15)

8. (a) Compare various interconnection medias.

   (b) How to achieve synchronization in multiprocessors computer. Discuss about distributed shared memory architectures. (5+10=15)

SECTION - E

9. Write short note on following:

   (a) MIPS R4000 pipeline.

   (b) Various RAID levels.

   (c) Instruction encoding.

   (d) Pipelining Vs parallelism.

   (e) Write back Vs Write through.

   (f) UNIX file system performance.

   (g) Virtual Memory.

   (h) Reducing cache miss penalty. (8×5=40)